Remarks

Reconsideration of this Application is respectfully requested.

Claims 1-17 are pending in the application, with claims 1, 14, and 16 being the independent claims.

Based on the following remarks, Applicants respectfully request that the Examiner reconsider all outstanding objections and rejections and that they be withdrawn.

Rejections under 35 U.S.C. § 102

Claims 1-5, 14, and 15 stand rejected under 35 U.S.C. 102(e) as being allegedly anticipated by U.S. Pat. No. 6,230,305 to Meares ("Meares"). Applicants respectfully traverse.

Meares discusses a computerized drawing system that enables a set of schematic diagrams to be created and modified. However, the system described by Meares differs from that of the present application, in that Meares is primarily concerned with using various overlapping circuits for different purposes, such as for tests, design, simulation, and the like.

The Meares system uses a single schematic diagram of a circuit under consideration, which is allocated into one or more layers. Those layers may be combined with other layers depending on the particular use of the schematic. These other layers may include, for example, parasitic capacitances, test inputs, and other auxiliary sub-circuits. The ability to combine layers allows for a plurality of different configurations, each of which shows a circuit or portions thereof together with the auxiliary sub-systems in a view that is suitable for use by different users of the system.

Thus, the single entry of elements into one or more layers in the Meares system is said to obviate the possibility of transcription error in creating the various views, which are created electronically once the data has been entered, making judicious use of the various layers.

The Examiner interprets the reference in Meares to "layers" as being "pages" (*see*, Office Action, page 3). Applicants respectfully submit that "layers" as used in Meares is different from "pages" as used in the present application. In Meares, each layer includes portions of a schematic which may or may not be shown depending on the use of the schematic. For example, a production engineer may need only the core circuitry displayed, while a test engineer needs to display the core circuitry in addition to test circuitry components (*see*, Meares, Table I). Thus, as shown in Fig. 4, a single display may include multiple "layers" which can be viewed all at once. In the present application, however, an IC layout may be represented by flat schematics, which display all of the details of the circuit. In most cases, a symbolic representation of an entire IC or portions of an IC require more than one page to display all the information. Thus, a single layer of the device may, when represented schematically, extend over several pages, which cannot be viewed at the same time. Therefore, Meares neither teaches nor suggests editing a schematic having a number of pages, as recited in claim 1.

Accordingly, Meares makes no mention of a multi-page schematic or of cutting and pasting a cut portion from one page of the multi-page schematic to another page. Thus, Meares neither teaches nor suggests, for example, "a module for cutting a selected portion of the schematic from any one of the schematic pages, each page displaying a viewable area of the schematic at a given time within the editor" or "a module for pasting

the cut portion of the schematic onto any one of the schematic pages," as recited in claim 1.

Furthermore, there is no teaching of "a module for connecting nets having the same label located on the same schematic page" as recited in claim 1. The Examiner states that "interconnections" in Meares are the same as "signal labels" in the present application (*see*, Office Action, page 4). However, as discussed in Meares, "interconnections" are the connections (reference 80 in Fig. 3) between all of the various components of the schematic, regardless of what the components are. Additionally, there is no indication in Meares of nets being labeled. Therefore, Meares neither teaches nor suggests "a module for connecting nets having the same label located on the same page" as recited in claim 1.

For at least these reasons, Applicants respectfully submit that claim 1 is patentable over Meares. Reconsideration and withdrawal of the rejection of claim 1 is respectfully requested.

Claim 2 recites "a module for searching objects within the schematic netlist." In addition to the reasons discussed with respect to claim 1, the Examiner has only identified the fact that when a modification is made on one layer and the same modifications are performed on other similar layers, the processor needs to determine which other layers are similar and contain the same elements in order to perform the same modification. There is no mention of a netlist in Meares, or a module for searching objects within the schematic netlist as recited in claim 2.

Regarding claim 3, the Examiner notes that data that could be input into the system could include interconnections. However, as discussed with respect to claim 1,

"interconnections" as used in Meares are different from "signal labels" as used in the present application. Further, Applicants submit that there is no teaching in Meares for any module for searching signal labels within a schematic netlist as recited in claim 3.

Regarding claim 4, the Examiner suggests that the symbols and their connections are tracked on the different layers. In fact, Meares teaches that each of the views may contain one or more schematic layers, each of which may contain information intended to be displayed for process and reviewing, and that such information may include schematic symbols and their connections. Thus, contrary to the Examiner's suggestion, there is no teaching that there is a tracking of the symbols or interconnections on the different layers, nor is there a list of symbols or interconnections. Further, as discussed with respect to claim 1, symbols and interconnections as used in Meares are not the same as signal labels as used in the present application. Notwithstanding the foregoing, Applicants submit that there is no teaching of a module which "provides a list of signal labels found on a preselected schematic page" as recited in claim 4. Indeed, there is no teaching at all of a list of signal labels in Meares. Additionally, although Meares discusses receiving assignment information to specify the layers in the schematic, this is not the same as preselecting a schematic page for which information is to be determined.

Similarly with regard to claim 5, there is no teaching in Meares that the module will provide a list of pages on which signal labels are found.

Regarding claim 14, and as discussed with respect to claim 1, Applicants respectfully submit that "layers" as used in Meares is different from "pages" as used in the present application. Meares neither teaches nor suggests editing a schematic having a number of pages, as recited in claim 14.

Regarding claim 15, the Examiner suggests that Meares teaches that a user may select any of the layers which comprise a displayed configuration and graphically and visually determine the contents of each of the layers within each of the configurations. This allegedly allows a user to determine the layer to which a particular component belongs. The Examiner alleges that this constitutes a teaching of project viewer software controls outputting schematic symbols enabling a user to view, trace, and search objects through the project net-list data. However, Applicants submit that there is no teaching in Meares that a computer readable medium contains "schematic page numbers, cell names, nets signal labels and segments" as recited in claim 14, from which claim 15 depends.

For at least these reasons, and for the reasons discussed with respect to claim 1, Applicants respectfully submit that claims 2-5, 14, and 15 are patentable over Meares. Reconsideration and withdrawal of the rejections of claims 2-5, 14, and 15 are respectfully requested.

Rejections under 35 U.S.C. § 103

Claims 6-9 and 17 stand rejected under 35 U.S.C. 103(a) as being allegedly unpatentable over Meares in view of U.S. Pat. No. 5,568,397 to Yamashita et al. ("Yamashita"). Applicants respectfully traverse.

Claim 6 depends indirectly from claim 1. As discussed above, Meares does not teach each and every element of claim 1. Yamashita does not overcome this deficiency.

Regarding claim 7, there is no teaching in either Meares or Yamashita of "a list of cells found on a preselected schematic page," as recited in claim 7.

Similarly, regarding claim 8, there is no teaching in either Meares or Yamashita that a cell may be searched using one of cell coordinates, name labels, or attributes, as recited in claim 8. Furthermore, Yamashita neither teaches nor suggests that the cell, whether a terminal or otherwise, could be searched by name label or attribute.

Regarding claim 9, there is no teaching in either Meares or Yamashita that "the module provides a list of schematic pages on which the cell is found," as recited in claim 9.

Regarding claim 17, there is no teaching in either Meares or Yamashita of a hierarchical structure "organized by schematic pages," as recited in claim 17. The cited reference in Yamashita merely discloses a memory structure in which pointers are used to access pages, terminals, and general device information. There is no indication that this is done in a hierarchical manner. Applicant submits that a hierarchical structure, as called for in the claim, requires that one terminal block will point to a plurality of other blocks of like kind. In this case, there is a one to one relationship through pointers, but the pointers only deal with ancillary information and do not deal with the kind of element required in a hierarchical structure.

For at least these reasons, and for the reasons discussed with respect to claim 1, Applicants respectfully submit that claims 6-9 and 17 are patentable over Meares in view of Yamashita. Reconsideration and withdrawal of the rejections of claims 6-9 and 17 are respectfully requested.

Claims 10-13 stand rejected under 35 U.S.C. 103(a) as being allegedly unpatentable over Meares. Applicants respectfully traverse.

Claim 10 recites "a module for eliminating extra pins or segment endings on a schematic." The Examiner admits that Meares does not teach editing pins or segments (*see*, Office Action, page 6). However, the Examiner states, without evidence, that it would be obvious to include this feature in an editing system. Applicants disagree, and request that the Examiner provide evidence that such a feature would be obvious.

Regarding claim 11, there is no teaching in Meares of "a module for rendering invisible the labels on a current active page or on all of the schematic pages," as recited in claim 11. At best, Meares discusses the addition or deletion of information from the layers. However, the deletion of information from the layers cannot, contrary to the Examiner's assertion, be equated to the concept of rendering the labels invisible. Rendering the label invisible merely means that the display of the label is not shown, but that it can be shown if it is later rendered visible. It does not mean that the label is deleted, which would require reentry and reconfiguration if later desired.

Claim 12 recites "a module for adding IN/OUT elements to pin segments." As admitted by the Examiner, Meares provides no such teaching. As indicated previously, Meares is directed to the concept of displaying schematic information in layers, and combining various layers to form different configurations to suit the user's needs. There is no discussion in Meares as to whether the elements attached to any schematic cells are input or output elements, or how to display such elements. As discussed with respect to claim 10, Applicants disagree with the Examiner's assertion that such a feature is obvious, and request that the Examiner provide proper support for the assertion.

Regarding claim 13, Meares neither teaches nor suggests a further module "for cutting a net on a schematic and providing a signal label to the two cut ends of the net,"

as recited in claim 13. The Examiner again contends without support that such a feature is obvious. Applicants disagree and request that the Examiner provide proper support for the assertion.

For at least these reasons, and for the reasons discussed with respect to claim 1, Applicants respectfully submit that claims 10-13 are patentable over Meares. Reconsideration and withdrawal of the rejections of claims 10-13 are respectfully requested.

Claim 16 stands rejected under 35 U.S.C. 103(a) as being allegedly unpatentable over Meares as modified by Yamashita, and further in view of U.S. Pat. No. 5,544,067 to Rostoker et al. ("Rostoker"). Applicants respectfully traverse.

Claim 16 recites "a process in a computer system for interactively viewing netlist data from a high level schematic including schematic page numbers, cell names, nets, signal labels and segments, the viewing process comprising generating the hierarchical structure of the schematic on one pane of a split screen, generating a selected part of the schematic on another pane of the split screen, generating a list of cell names and a window on the screen, and generating a list of signal labels in a window on the screen.

The Examiner suggests that Meares teaches the display of layers on a display including corresponding layer information such as symbols and/or connections. However, as discussed above, Meares does not teach using schematic page numbers, generating hierarchical structures, or generating a list of cell names or signal labels. Rostoker does not overcome these deficiencies in Meares.

Instead, the Examiner relies on Rostoker, and in particular Figs. 14 and 15 thereof, in support of the argument that structures could be displayed on one pane of a

split screen and the schematic on another pane of the split screen. However, this is not what is claimed in claim 16. What is claimed, rather, is generating the hierarchical structure of the entire schematic on one pane and a selected part of the schematic on another pane.

Rostoker displays no schematic at all. Rather, in various panes, a high level program is used to define relationships between structures, as well as specific windows which display the resources available and which have been utilized in terms of the design concept. This is very different from the display of a hierarchical structure on one pane of a split screen and a selected part of a schematic on another pane, as recited in claim 16.

For at least these reasons, and for the reasons discussed with respect to claims 1, 6-9 and 17, Applicants respectfully submit that claim 16 is patentable over Meares as modified by Yamashita and further in view of Rostoker. Reconsideration and withdrawal of the rejection of claim 16 is respectfully requested.

Conclusion

All of the stated grounds of objection and rejection have been properly traversed, accommodated, or rendered moot. Applicants therefore respectfully request that the Examiner reconsider all presently outstanding objections and rejections and that they be withdrawn. Applicants believe that a full and complete reply has been made to the outstanding Office Action and, as such, the present application is in condition for allowance. If the Examiner believes, for any reason, that personal communication will expedite prosecution of this application, the Examiner is invited to telephone the undersigned at the number provided.

Prompt and favorable consideration of this Amendment and Reply is respectfully requested.

Respectfully submitted,

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